AMENDMENTS TO THE SPECIFICATION

Please amend the initial paragraph that sets forth the cross-reference as follows:

CROSS-REFERENCE TO RELATED APPLICATION

This application claims priority of a provisional Application filed September 19, 2003, Serial No. 60/504,127 ~~Not Yet Assigned~~, the entire contents of which are incorporated herein by reference.

Please amend paragraphs **[0007]**, **[0023]**, **[0056]**, **[0076]**, **[0110]** as follows:

[0007] There have been prior proposals for analysis of crosstalk induced delay. R. Arunachalam, K. Rajagopal, and L. Pileggi,[[.]] Taco, "Timing analysis with coupling". *Proceedings of the Design Automation Conference*, pages 266-269, June 2000 teach that static timing analysis (STA) can be used to calculate delay while accounting for effects of switching aggressors using a heuristic-based Miller factor, which is applied to coupling capacitance before it is grounded. This approach is believed to be too conservative and inaccurate to be successfully used for modern design constraints. Another approach is based on computation of a *noisy transition* - transition in the presence of switching aggressors, and using it for determining new slews and delays. In several studies the linear superposition principle was applied to the *nominal transition* with a noisy waveform on the victim net computed separately. See, F. Dartu, *et al.*; R. Arunachalam, *et al.*; and P. D. Gross, R. Arunachalam, K. Rajagopal, and L. Pileggi, "Determination of worst-case aggressor alignment for delay calculation", *Proceedings of the ICCAD*, pages 212-219, November 1998. The nominal transition is computed using a linear Thevenin model for the victim driver with all aggressors kept quiet. The alignment between nominal transition on the victim and transitions on the aggressors was chosen based on noise pulse width and height. However, since the noise wave was computed for a quiet victim driver and not a switching one, the alignment used in the mentioned studies could be inaccurate.

[0023] **Figures 6A-6B** are illustrative drawings that show, conceptually, the conversion of a stage in a design to a simpler circuit suitable for crosstalk analysis in accordance with an embodiment of the invention.

[0056] The circuit 500 of **Figure 5**, is configured for calculation of fast transitions on first order aggressor net 502 (agg1). The neighbors of aggressor net 502 are victim net 504 and (victim) and second order aggressor net 506 (agg1_1). Parasitic capacitances C_P couple aggressor net 502 to victim net 504 and couple aggressor net 502 to second order aggressor net 506. Nets (not shown) that are more remote from aggressor net 502 are assumed to have a minor impact of results and are thus decoupled. Aggressor net driver 508 is coupled to drive aggressor net 502. Respective drivers for victim net 504 and second order aggressor net 506 are replaced with respective resistances R_{h2} and R_{h1} that are connected to ground, and the receivers are replaced by ground capacitors to model their respective gate capacitance. The holding resistors are found from the cell library, and they approximate the weakest holding driver of the respective net.

[0076] **Figures 6A-6B are** [[is an]] illustrative drawings ~~drawing~~ to show, conceptually, the conversion of a stage in a design to a simpler circuit suitable for crosstalk analysis in accordance with an embodiment of the invention. **Figure 7** ~~**6B**~~ is a two-dimensional (2D) current table representing the non-linear ViVo current model 626 of a real driver 608 of **Figure 6A**. In accordance with one inventive aspect, original stage 600A is converted to a simplified stage represented as a current model stage 600B. Stage 600A includes a victim net 602 and aggressor net 604. The victim and aggressor nets are coupled through parasitic capacitances C_P. Victim net driver 606 is connected to the victim net 602 at node 613. In this example, the victim driver 606 includes multiple internal components 608-612. Each internal component 608, 610 and 612 is a channel-connected component (CCC), each including transistors connected to each other by their drains or sources. Such partition of a circuit into CCCs allows more efficient analysis used during static timing and noise analyses because a driven CCC, 608, has negligible impact on noise or delay on its respective driving CCC, 610, 612. The aggressor net 604 is grounded using a holding resistance R_h. The holding resistance is pre-characterized for each gate and both logical stages and stored in a cell library, such as .cdB library used by a noise analysis tool such as CeltIC produced by Cadence Design Systems, San Jose, California. The holding resistance can be computed (during the library characterization stage) using Spice circuit simulator. A first receiver 614 has a first receiver input 616

and a first receiver output 618. A second receiver 620 has a second receiver input 622 and a second receiver output 624.

[0110] In accordance with one inventive aspect of an embodiment of the invention, $V_k(t)$ only need to be computed once and then can be re-used for all alignment vectors τ similar to the current responses $I_k(t)$. Once $V_{i,k}(t)$ are computed, for each alignment vector τ the calculation of noisy transition at the receiver due to noisy transition on victim driver requires one convolution, $L\{H_{j,o}L[x_o]\}$. The voltage response at the receiver is then obtained from a superposition with time shifted known voltage responses from aggressors.